

# PRONANO



Contract NMP2-CT-2005-515739

## PRONANO

Technology for the Production of Massively Parallel Intelligent  
Cantilever - Probe Platforms for Nanoscale Analysis and Synthesis

Instrument: Integrated Project  
Thematic Priority: NMP

### Month 48 Periodic Activity Report Public Summary

Period covered: from 01-04-2008 to 31-03-2009  
Start date of project: 01-04-2005

Date of preparation: 13-05-2009  
Duration: 5 years

Project coordinator:  
Project coordinator organisation:  
Revision:

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v20090513

## **Publishable executive summary**

After realization of components as probes, packages, electronics and scanning stage during the first two years, followed by the assembly of a first complete demonstrator system in the third project year leading to a comprehensive insight in the addressed massively parallel cantilever technology, the fourth year of PRONANO was dominated by the implementation of improvements based on testing and evaluation of the system and significant stepping forward in increase of integration.

The major obstacles for parallel operation of several cantilevers within a multi-cantilever array as electrical and mechanical cross-talk were addressed and solved by the realization of novel probes with adjusted layout and optimization of electronics. Simultaneously, parallel surface imaging with several cantilevers has been established by numerous demonstrations including measurement with overlapping images by two groups. The cantilever control electronics based on discrete components has been scaled to 32 channels and integrated into the overall system.

The integration of the cantilever control electronics into ASICs proceeded by the realization of all electronics blocks whereas the analogue, ADC- and DAC-components were realized in form of concrete ASICs while the digital components were realized as FPGA code for evaluation. The integration of realized ASICs into the overall electronics has been started and will replace the currently applied electronics within the first months of the coming period. Simultaneously, the design of fully integrated multi-channel cantilever control ASICs has been started as basis for controlling the operation of massively parallel cantilever arrays.

The industrial application of the cantilever based parallel surface measurement has been driven forward by the preparation of state-of-the-art test patterns for evaluation of mask metrology, by the preparation of the measurement setup for 150mm samples of the end-user and the demonstration of measurements within the vacuum chamber of a mask repair system.

Although, the realization of first 2-dimensional cantilever array probes with integrated through silicon interconnections encountered the most severe difficulties, significant progress in this field can be reported, as well. A first series of especially tailored SOI-wafers with pre-manufactured poly-silicon through wafer interconnections could be realized in co-operation with an external partner. These wafers will serve as basis for the fabrication of first demonstrator probes which are expected to be finalized at the beginning of the coming project period. The fabrication scheme has been analyzed and first tests on packaging of these probes were carried out. The realization of a dedicated package for 2-dimensional arrays with through chip interconnections was started.

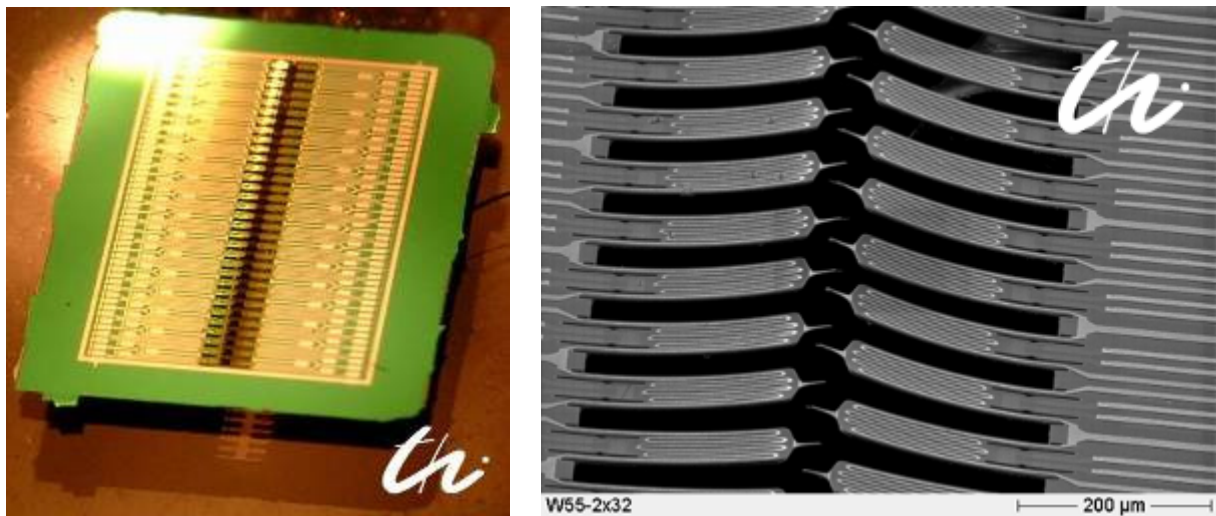
For dissemination of project results a joint participation at an international scientific conference was organized and several scientific publications were filed. The web-based course on micro-cantilever technology was extended by an in-depth module explaining the mechanics of cantilevers.

### **WP1**

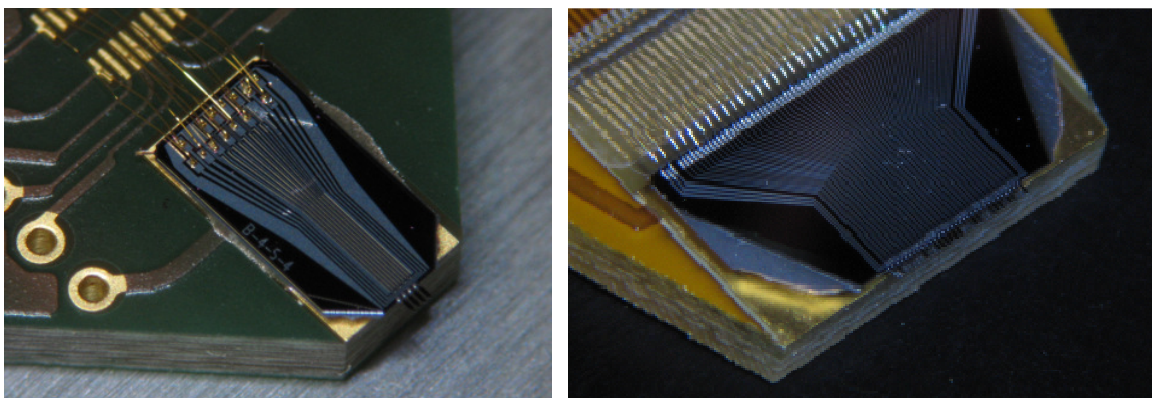
During the reporting period the WP1 partners Nanoworld (1) and TUI (18) studied, modelled, developed, realized and characterized parallel SPM arrays based on self actuated piezoresistive cantilevers. To fulfil the project targets, the fabricated devices have been analysed and characterized in-house after fabrication, closing the feedback loop between design and fabrication. Parallel proximal scanning with overlapping images was successfully demonstrated in WP2/WP3 using self-actuated piezoresistive cantilever arrays fabricated in WP1. Shallow junction implantation technology for highly sensitive 2-dimensional electron gas (2DEG) quantum confinement piezoresistive read-out sensor was established by the partner FZD (11). The first generation of parallel SPP chips have been integrated into the nano-measurement

machine of partner SIOS (12) and first test measurement were performed showing 0.2nm resolution in vertical direction.

During the reported time TUI developed a SPICE based equivalent-circuit model for identification and quantification of crosstalk effects in self-actuated cantilevers. This model includes cantilevers with piezoresistive read-out and bimorph actuators based on implanted heaters. TUI-SPICE-Model was successfully implemented and different sources of cross-talk have been identified, simulated and quantified. Novel methods for crosstalk reducing employing additional shielding and improved actuator-sensor separation have been successfully implemented by Nanoworld and TUI. The revised design of the 1<sup>st</sup> generation SPM-arrays has been realized in order to supply to the partners of WP2 and WP3 probes for characterization and demonstration tasks (Fig. 0.1 and Fig. 0.2). Investigation performed by WRUT (13) and SIOS (12) have shown that the electrical crosstalk is negligible and does not hinder the application of cantilevers with bimetal actuator and piezoresistive read-out.



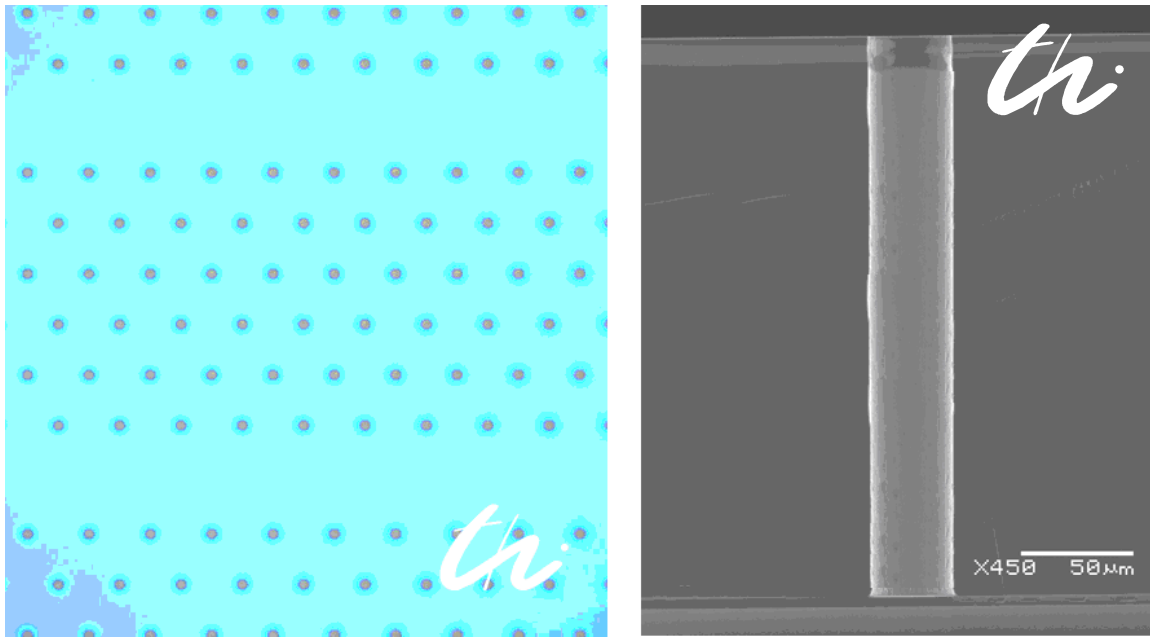
**Figure 0.1** Two-dimensional SPP array with 2x32 cantilevers with planar wiring and significantly reduced cross-talk, developed by TUI (left: optical, right: SEM picture)



**Figure 0.2** Packaged 1-dimensional cantilever array probes realized by Nanoworld (left: 1x4 array, right: 1x32 array)

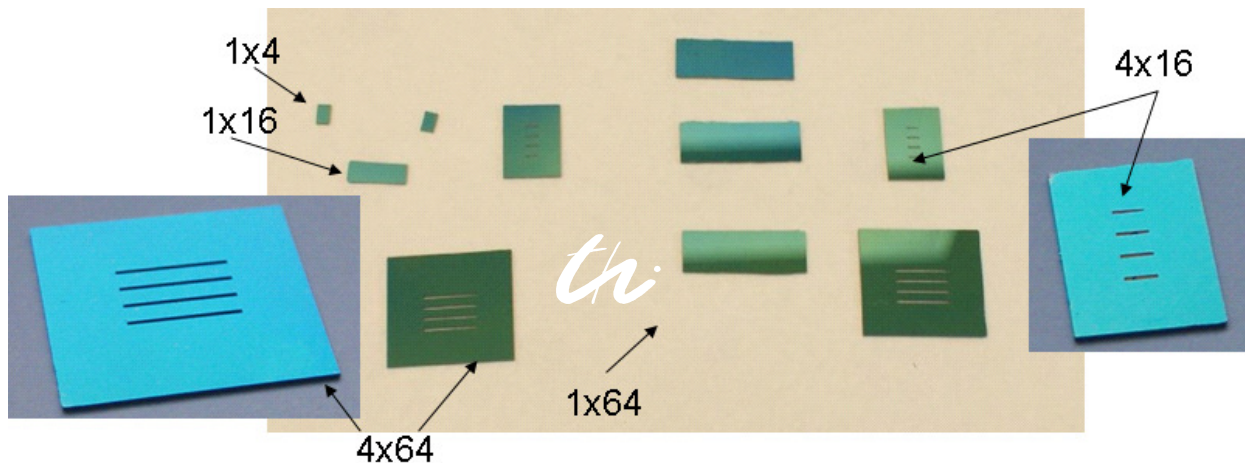
A major issue of the reporting period was the realization of the second generation of probes with vertical interconnections. The fabrication of the SOI substrates with through silicon vias (TSV) by the external partner IceMOS was significantly delayed (12 months). Facilitated by TUI, IceMOS was able to deliver first SOI wafers with TSV in the beginning of February 2009 (Fig. 0.3). The fabrication of first SPP arrays of the second generation incorporating vertical

interconnection technology is currently in progress and further wafers with pre-manufactured interconnections are currently produced by IceMOS.



**Figure 0.3** SOI wafers with vertical interconnections; a) microscopic view of the field of vias, b) SEM picture of the vertical cross-section of a via.

TUI has developed a deep silicon plasma etching process as basis for the fabrication of the 2<sup>nd</sup> generation of cantilever array probes. The layout and technological fabrication sequence of the second generation of SPP arrays was investigated and applied to technology pre-studies. A series of demonstrators mark the result of these studies (Fig. 0.4). TUI spent enormous efforts on the deep silicon etching in order to establish this technology.



**Figure 0.4** Second generation 1-D and 2D test chips, realized by deep plasma etching based on gas chopping technology.

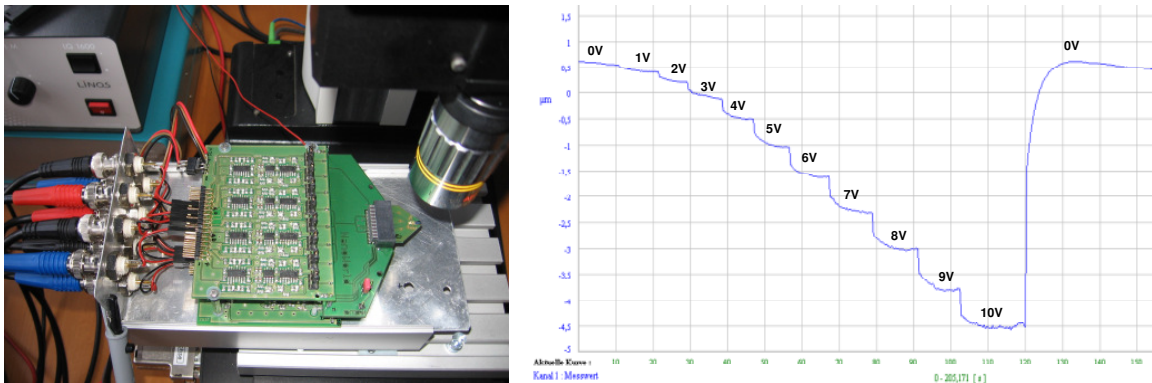
### WP3

Integration and testing of now available one dimensional cantilever arrays with up to 32 probes was at the centre of this reporting period's development. We also acquired first images of industrial relevant specimen demonstrating state-of-the-art performance of PRONANO probes.

Packaging of the 1x32 probe arrays, which is a crucial part of system integration, required a new and optimised packing concept, because previous designs had to be adapted to the revised probes layout and electrical cross-talk within the package should be reduced. As new approach, low temperature cofired ceramic packages (LTCC) based on the new design were manufactured by TUI. Measurements confirmed that cross-talk from which a previous design suffered has been significantly reduced. If needed a further reduction could be achieved with a design based on new connector and a new pin out.

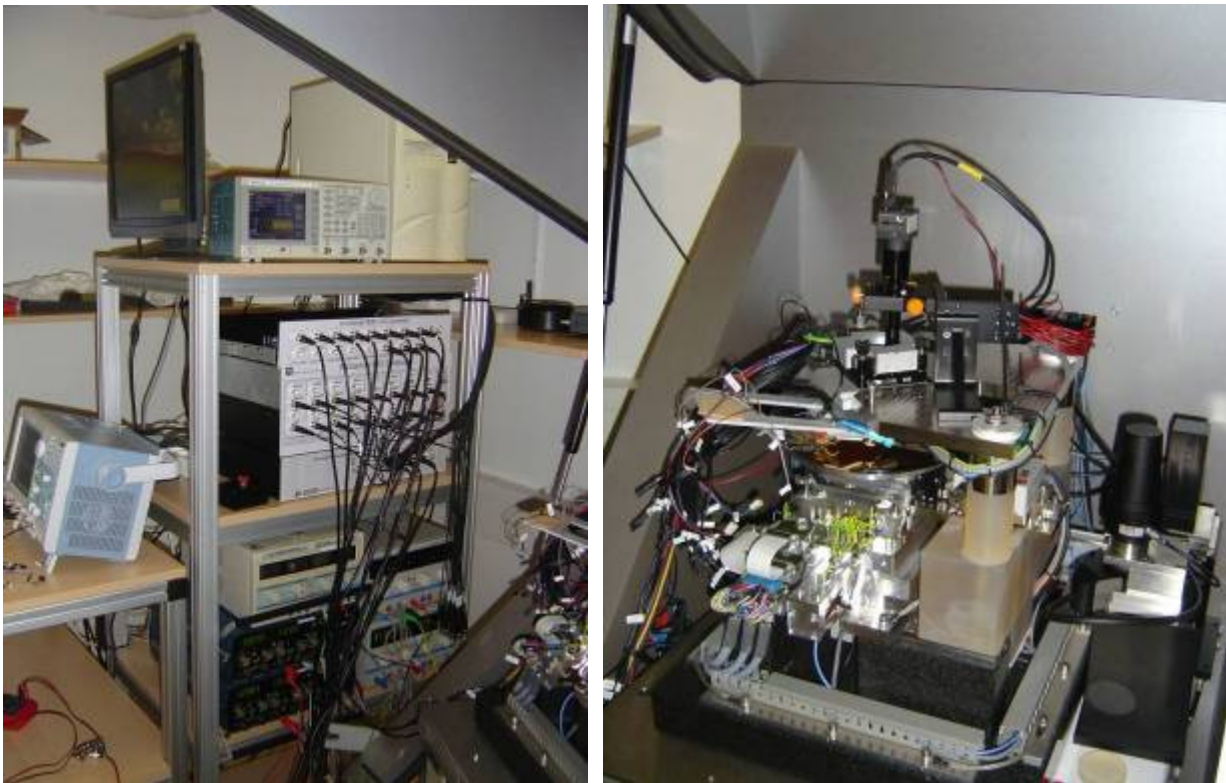
TUI also addressed the packaging of two dimensional arrays that raises new challenges. Two different approaches for the package of 4x16 cantilever arrays are studied. Whereas the first approach is based on a LTCC in multilayer technology, the second approach uses post-fire ceramic avoiding the shrinkage of the LTCC process. Fabrication of these packages has been started.

For the measurements mentioned above, Nanoworld's test setup has been extended with a laser-vibrometer which is capable of high resolution static and dynamic cantilever deflection measurements. This system was also used for test of 4x1 probe arrays and for the measurements of the actuation efficiency as a function of cantilever thickness.

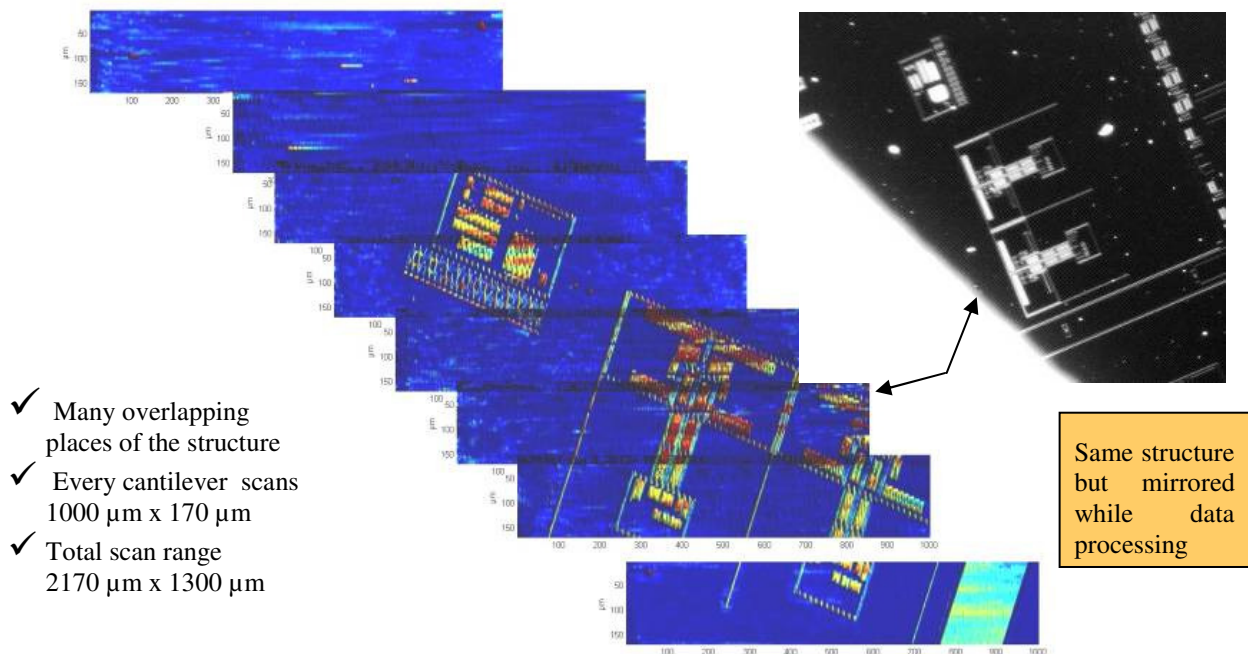


**Figure 0.5** Vibrometer measurement system with 8-channel analogue front-end electronics and mounted 1x4 cantilever array (left) and measurement of static deflection with internal bimorph actuator (right).

The results for 1x32 probe arrays match with similar results from tests carried out by SIOS. Their, now to 32 channels extended and improved test bench, which is adjustable for different cantilever response times was used to image the surface of test specimen. Large scans with overlapping imaging area were demonstrated, but it was not possible to engage a large percentage of the probes since the fabricated probe array still suffer from a large variation of the individual probe Z-level. Images were also acquired on test wafers provided by Infineon and Vistec. These test specimen feature surface structures which are relevant for the semiconductor industry.



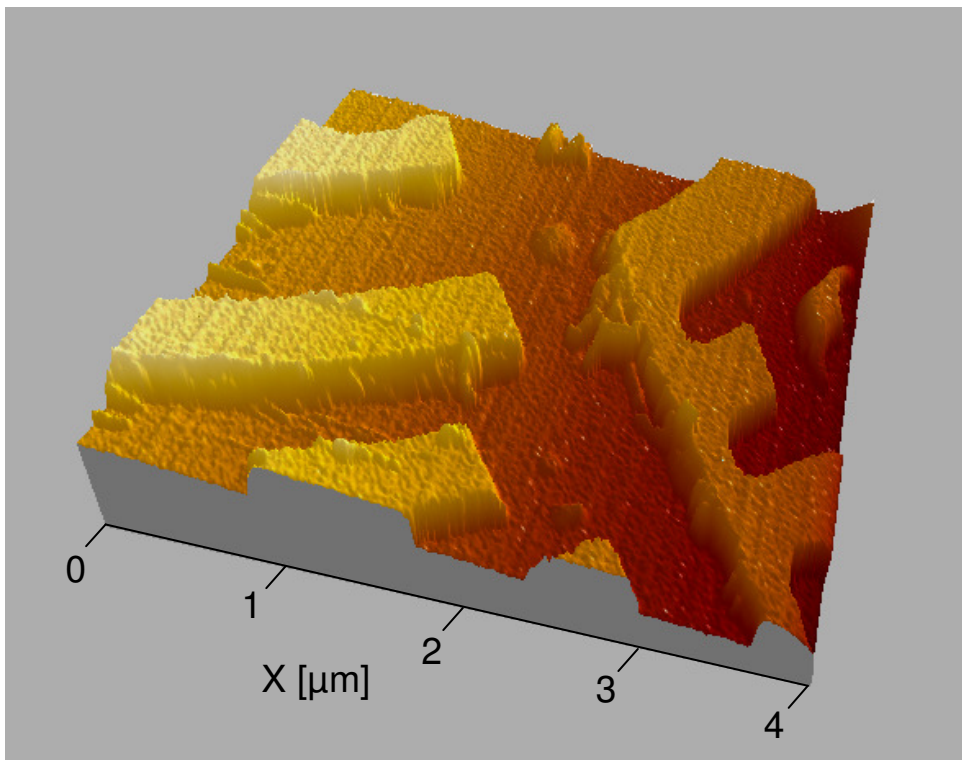
**Figure 0.6** SIOS surface scanning test-bench with integrated PRONANO cantilever array probe head for parallel surface scanning experiments (right) and multi-channel cantilever control electronics (left)



**Figure 0.7** Parallel surface scanning with eight cantilevers of the same cantilever array

The extension of the control electronics to 32 channels was driven by WRUT based on a hybrid design including ASIC preamplifiers combined with more conventional control modules. The system also has an enhanced immunity to the crosstalk of the probe arrays.

In contrast to the tests with multiple probes NaWoTec used single cantilever probes and concentrated on high definition imaging which is needed for metrology applications. After solving several serious technical issues, high quality images of photomasks for chip fabrications have been collected. These photomasks are very difficult to image due to the very high aspect ratio and the complexity of the mask patterns. Nevertheless high image resolution and low image aberrations of these results are similar to commercial state-of-the art systems indicating the full potential of PRONANO cantilever probes. The photomask repair pilot application also requires to operate the probes within the vacuum environment of the electron microscope of the mask repair tool. First in-situ measurements were performed with the AFM integrated into the repair tool. In-situ imaging quality was found to be sufficient to gather the crucial topography data which are needed to control the repair of photomask defects.



**Figure 0.7** AFM image (unprocessed raw data) of test grid acquired in-situ with the tool chamber under vacuum ( $\approx 5E-7$  mbar). The height of the pattern is 85nm.

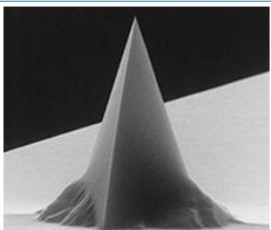
## WP4

The 4<sup>th</sup> Pronano workshop was organized in collaboration with the international workshop « Nanomechanical Cantilever Sensors » on May 19-21, 2008 at Mainz, Germany (<http://www.mpip-mainz.mpg.de/symposium/nmc2008/index.php>). The Pronano partners presented the results of the project achieved so far by 2 poster presentations and 2 oral presentations. Totally 140 participants from Europe and US participated in the workshop.

**Figure 0.8** Presentation of Prof. T. Gotszalk at international workshop «Nanomechanical Cantilever Sensors», May 19-21, 2008 at Mainz.



A second on-line course, elaborated by a team of Pronano partners, is available on the e-learning platform MyTeacher (<http://www.cerfi.ch>). The course is on “**Mechanics of Microcantilevers**”. Learning time is about 1 hour. Participation is free of charge and needs a personal password. Also available: 1<sup>st</sup> Pronano on-line course “Introduction to Microcantilever Applications”.

Silicon	PRONANO
Material Matters	
<p>Silicon is a classical metalloid and has many industrial uses, most significantly in semiconductor devices, integrated circuits and microchips. Silicon is also a widely used material and the basis for MEMS fabrication either as a substrate for material growth or to form components.</p> <p>Silicon has a regular crystal structure with physical properties, such as stress and strain, strongly dependent on the crystalline orientation. The crystal structure makes silicon ideal for microcantilever sensors based on resonance operation with high natural frequency and high Q-factor. Integrated piezoresistive cantilevers are typically realized with p-type doping due to higher piezo- coefficients in the [110] direction</p>	 <p>Image Courtesy of Nanoworld</p>
<p><i>Material Properties of Silicon, as other materials in this section, are included in the final slide</i></p>	<p><b>Silicon Nanotip:</b> Scanning probes can be fabricated with nanoscale tips to interact with atomic surfaces with high resolution. Tips can be fabricated using a number of technique and given various properties for different types of imaging.</p>

**Figure 0.9** Example page of the new web-based course module "Mechanics of Microcantilevers"

8 presentations at conferences and 3 scientific publications have been done by the consortium partners during reporting period and further publications are under preparation. They contributed to the successful knowledge transfer from inside the project to the wider scientific community.